Effect of Vth shifting in CMOS Transistors under radiation conditions when applying OBT: A case study

Pablo Petrashin
Laboratorio de microelectrónica
Universida Católica de Córdoba
Cordoba, Argentina
ppetrashin@gmail.com

Walter Lancioni
Laboratorio de microelectrónica
Universida Católica de Córdoba
Cordoba, Argentina
walter.lancioni@gmail.com

Agustin Laprovitta
Laboratorio de microelectrónica
Universida Católica de Córdoba
Cordoba, Argentina
agustin.laprovitta@gmail.com

Fortunato Dualibe
Faculté polytechnique de Mons (FP)
Service d'électronique et de microélectronique (SEMi)
Mons, Belgium
Fortunato.DUALIBE@umons.ac.be

Juan Castagnola
Laboratorio de microelectrónica
Universida Católica de Córdoba
Cordoba, Argentina
juanluiscastagnola@gmail.com

***Abstract*— In this work, we explore the ability of Oscillation-Based Test (OBT) for testing OTA-C filters (Operational Transconductance Amplifier – Capacitor) based circuits under radiation conditions. We adopt an OTA as a case study for testing. The effectiveness of the strategy is qualified by means of fault simulation. It is known that there are several parameters moving when submitting a circuit to radiation, such as carrier's mobility or Threshold Voltage (VTH). This paper presents an exploring experience when trying to test a circuit under environmental radiation conditions. The idea is to observe the oscillation condition for OBT under a radiation-dependent oscillating parameter in order to obtain certain usage limits for the OBT technique, among some other useful conclusions.**

***Keywords*— OBT, CMOS Dosimeters, Radiation Dosimetry, Temperature Compensation.**

I. Introduction

The Oscillation-Based Test is a Design-for-Test technique that can be used either in off-line testing or as the core of the so-called OBIST (Oscillation-Based Built-In-Self-Test). The basic idea is to convert the Circuit Under Test (CUT) into an oscillator during the test phase, as has been extensively discussed for several circuits (operational amplifiers, filters, data converters) [1-3]. During the test, a feedback loop is added to the CUT to produce self-sustained oscillations. This feedback can be globally applied to the overall CUT or to a part of it. Faulty behavior is then indicated by deviations in the frequency and/or the amplitude of the oscillations, with respect to the values of these test attributes under fault-free conditions [2]. OBT avoids the problem of test vector generation, requires relatively simple measurements and generally does not demand strong circuit modifications during the testing phase. These characteristics make OBT an appealing strategy.

The implementation of OBT depends hardly on the characteristics of the system under test. The oscillator has to be designed and implemented based upon several considerations, such as the characteristics of the system, the possibility or not for partitioning the CUT, the observable outputs, the analog or digital nature of the signal, etc. Consequently, the application of this strategy to each new class of circuits becomes a challenging task.

The test of low-order continuous-time filters by OBT can be found in [3-5]. In these papers, simple and relatively common topologies are adopted, and analytical expressions for the oscillation conditions are obtained. Huertas et al. [6], [7], [8] and Kac and Novak [9] have studied the application of OBT to high-order switched-capacitors filters designed as cascade of first and second order sections. These authors propose to divide the filters in low order sections and to test separately each one. The main objection to this approach is that the extra circuitry needed for switch the circuit from the test mode into normal mode may cause not tolerable degradations in the signal. On the other hand, it cannot be extended to filters that may not be divided in low-order sections. Some deeper studies have been made in [10-11].

In this work, we explore the ability of OBT for testing OTA-C oscillator under radiation environment, in order to find the limits within the technique can be applied. Adopting a second-order structure as a case study, we present a simple scheme that allows an easy visualization. The evaluation of the test quality is made by means of fault simulation.

II. Effects of radiation on VTH

There are basically two types of radiation: particle (typically neutrons or protons) and photons (X or Gamma radiation) [12], [13]. The latter is the one received when a cancer treatment or diagnosis is made. In these cases, it is common practice to measure the Total Ionizing Dose (TID) in Gray (Gy) [14], which is defined as the absorption of one Joule of radiation energy per kilogram of matter.

In a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) integrated circuit, electron-hole pairs are generated in the oxides and insulators due to ionizing radiation [13]. This effect could lead to the degradation and failure of the device [15], but it is also feasible to use it to determine the radiation dose through the TID measurement. In these circuits, some short-term single-event effects, called Single Event Effects, or SEEs, occur, which are present for a short time interval, causing momentary changes in device properties. However, there are other effects that can become permanent [16], [17]. The latter, called long-term effects, constitute the operating principle of this proposal.

When radiation is detected using silicon circuits, the change in threshold voltage (VTH) with the radiated dose has been commonly used as a measurement parameter. One of the main problems when using MOS circuits for dosimetry is the displacement of VTH due to temperature, an effect that can lead to incorrect readings [8]. While this is not a serious problem for high dose measurements, special care must be taken to avoid this effect when measuring low radiation doses. In the literature there are different ways to approach the problem of thermal compensation, either with elaborate circuits or configurations [5], [6], [10] or at the cost of external processing [14]. All of these approaches involve the over-allocation of circuit resources, and their respective impact on integration costs. Some authors have made deep studies measuring the VTH variation when submitted to radiation [18, 19], allowing to use the results for predicting behavior under certain conditions. From [19] we can interpolate the data for the adequate biasing voltage. This can be seen in figure 1.

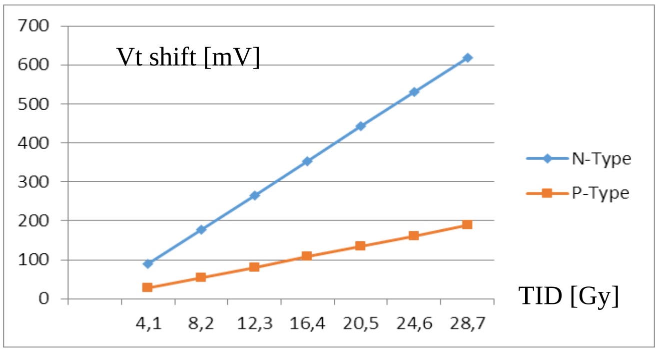

Figure 1 Vth shift for nMOS and pMOS. Interpolated data for different dose from [16].

These data will be used for further simulations. It can be seen that besides other things, VTH shifting depends strongly on the type of CMOS transistor (nMOS or pMOS).

III. Circuit Under Test

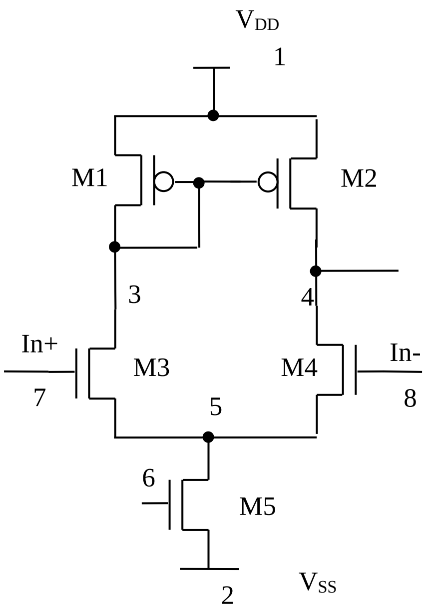

Figure 2. Transconductor under test

When designing analog circuits, the usage of Gm-C OTAs allows the fabrication of low cost and low area continuous time filters, among other circuits. Many of the OTA-based structures use only OTAs and capacitors and, hence, are attractive for integration. Additionally, the component count of these structures is usually very low, decreasing the area cost [20] and making them suitable for monolithic circuit structures. In order to explore the ability of OBT for testing Gm-C structures, a simple OTA is adopted as a case study. The transistor-level schematic is shown in Fig. 2, while the transistor sizing is shown in table 1.

Table 1. Transistor sizing for the circuit under test

Device Name	W/L (µm)
M1, M2	12/2
M3, M4	12/7
M5	8/2

IV. OBT Implementation

In order to perform OBT on the circuit, the CUT must be placed into a self-sustained oscillation condition. The implementation of the OBT strongly depends on the characteristics of the system under test. The oscillator should be designed taking into account several considerations, such as the characteristics of the whole system, the possibility of partitioning the CUT, the observable outputs, the analog or digital nature of the signal, and others. Consequently, the application of this strategy to each class of circuits requires special attention.

An OTA may be placed in oscillation using several oscillator configurations. One way is to use it in a pass-band filter, which in turn is positively fed back so as to oscillate. One way to do so is shown in Figure 3. The conventional OBT procedure is applied, whereby once the circuit is switched into oscillation, its output voltage amplitude and oscillation frequency are compared to those of the non-faulty output.

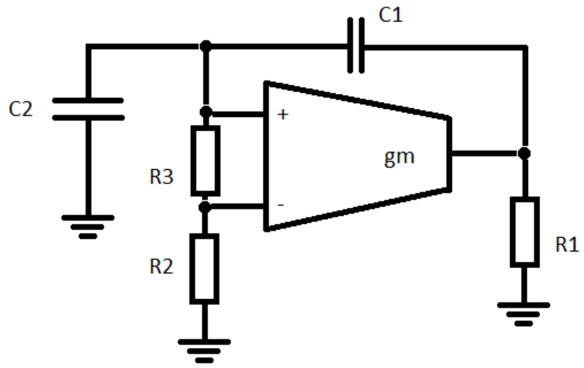

Figure 3. Block diagram of the circuit connected as oscillator.

The frequency output for this circuit is given in (1)

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1 C_2 R_1 (R_2 + R_3)}} \quad (1)$$

V. Fault Modelling

Traditionally, the efficiency of OBT has been evaluated at structural-level by using single-catastrophic and single-deviation fault-models. In this way, it is possible to use the well-known metric called fault-coverage for qualifying the test.

In this work, we focused our attention on catastrophic faults at both, device and circuit level. In this way, we preliminary evaluate the efficiency of OBT for the faults that may cause severe failures in the circuit.

Since the layout of the circuit is not available, an exhaustive fault list from the schematic is generated, considering only catastrophic faults. This fault list includes all possible open and short faults of transistors, with only the exception of gate contact open fault. We consider short faults at the circuit level rather than only shorts at the transistor level in order to take into account all probable faults. Additionally, this procedure allows further comparisons with results reported by other authors.

The CUT has 8 nodes, with nodes 6, 7 and 8 being gate input contacts. The nodes are numbered in Figure 1, with the schematically redundant ones listed in Table 2. The reference node and its schematically redundant sub-nodes are connected at the same potential, making it impossible to detect behavioral differences between them. In this sense and taking into account all redundant nodes, 527 potential short circuit faults are possible, whereas 26 open circuit faults can be considered when only drain and source contacts on the transistors are included in open circuit analysis.

Fault simulations are carried out using LTSPICE using the AMI C5 process.

Table 2. List of main and redundant nodes

Reference node	**Redundant nodes**
1	M1_S, M2_S
2	M5_S
3	M1_S, M1_G, M3_D
4	M2_D, M4_D
5	M3_S, M4_S, M5_D
6	M5_G
7	M3_G
8	M4_G

Open faults are modeled by a 10 MΩ resistor while short circuit faults are modeled by a 10 Ω resistor; choices which are substantiated in [10]. It is assumed here that a fault is detected when f_{usc} or V_{pp} falls outside of a tolerance band of ±5% from the nominal values simulated in the TT corner.

Table 3. Passive circuit component values in all simulations

R1	100kΩ
R2	100 kΩ
R3	100 kΩ
C1	20pF
C2	20pF

Assuming VTH variations as in figure 1, the graphic shown in figure 4 can be drawn.

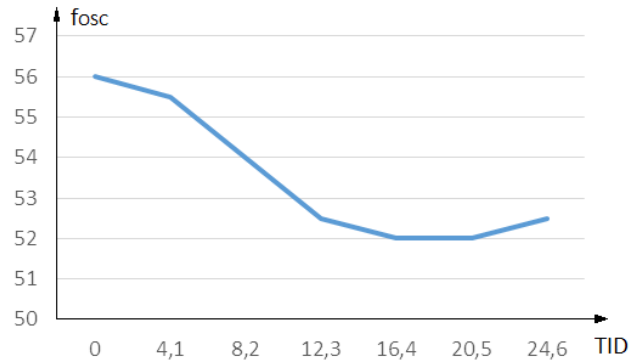

Figure 4. Representation of output frequency as a function of TID

As it can be seen in figure 4, the oscillation frequency shifts down as radiation dose (TID) increases, showing that after approximately 8.2 Gy the circuit falls out the 5% of the nominal value. The effect is similar to move nMOS toward the FAST zone and pMOS toward the SLOW zone (FS corner).

It is easy to realize that the application of the traditional OBT for untuned filters [21] in this case, may show an out-of-tune device as being defective, even if it still works well for its intended purpose.

Because of this fact, the implementation of efficient OBT based tests in such filters results impracticable. To overcome this problem, we´ve proposed an improved OBT method that performs a relative comparison between two oscillation frequencies that could be applied in cases such as the depicted here [21].

Different configurations for the oscillator must be tested in future works, to show how circuits with different sensibility [21] may show also different behavior under radiation conditions.

VI. Conclusions

An OBT scheme has been applied to an OTA-C band pass filter. For evaluating OBT, we adopted catastrophic fault models at both, device and circuit level.

It has been shown that the traditional OBT methodology can be used within a narrow margin when applying it in a radiation environment. This phenomenon can be improved if using a relative frequency comparison over the process corners.

In future works, we will address different configurations for the oscillator, given the fact that different sensibility may also show different behavior under radiation conditions.

Simulation validation have been carried out for a given fault in several topologies assuming the TT process corner. Future work will also include a comprehensive test campaign that includes all faults under all process corners, along with an analysis of the circuit sensitivity to the values of the off-chip connected resistors and capacitors. This latter will allow the DFT designer to choose the best external component values.

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